REMARKS

In accordance with the foregoing, the specification and claims 1, 3, 6-9, and 11 have been amended. New claims 12, 13, and 14 have been added and present no new matter.

Thus, claims 1-14 are pending and under consideration.

OBJECTION TO THE TITLE:

In the Office Action, at page 3, the title was objected to as not being descriptive. As suggested by the Examiner, the title has been replaced.

CHANGES TO THE SPECIFICATION:

The specification has been reviewed in response to this Office Action. Changes have been made to the specification only to place it in preferred and better U.S. form for issuance and to resolve the Examiner's objections in the Office Action. No new matter has been added, as there is support for the changes throughout the specification and drawings as originally filed.

CLAIM OBJECTIONS:

In the Office Action, at page 3, claims 1, 6, 7, and 11 are objected to because "likelihood of branching" is unclear to the Examiner and because of other various informalities.

In response, the claims have been amended to improve clarity and antecedent basis support.

Accordingly, it is respectfully requested that the objections to the claims be withdrawn.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at page 4, item 9, claims 1-11 have been rejected under 35 U.S.C. § 103(a) in view of U.S. Patent No. 6,550,004, issued to Henry *et al.* (hereinafter, "Henry") and U.S. Patent No. 6,108,775, issued to Shiell (hereinafter, "Shiell"). The rejection is traversed and reconsideration is requested.

The Examiner has alleged that Henry discloses all elements of independent claim 1, except a branch destination buffer. According to the Examiner, however, Henry discloses a buffer, but the alleged buffer of Henry is not a branch destination buffer which stores therein a branch destination address or predicted branch destination address of an instruction. The Examiner has alleged that Shiell has disclosed the use of a dynamic branch predictor that is a

branch destination buffer or branch target buffer that stores a branch destination or target address of an instruction and is indexed by tags.

Henry is directed toward a branch predictor apparatus. The apparatus includes a static predictor that makes a static prediction of whether a conditional branch instruction will be executed, based on a test type of the branch instruction. The apparatus also includes two dynamic predictors. *See* Henry, column 8, lines 8-10. The dynamic predictors include history table X and history table Y, respectively, which are coupled to index generation logic 312 and 314, respectively. *See* Henry, column 8, lines 31-35. The index generation logic 312 is responsible for generating an index.

The present invention is directed to an apparatus for branch instruction prediction. The apparatus includes, but is not limited to, a history register which stores a history of previous branch instructions, an index generation circuit, and a history table which stores a tag, which is a portion of the instruction address, and a count value to assist in determining instruction branch prediction. *See* Specification, page 6, lines 13-34. Thus, to compare a portion of the instruction address corresponding to the tag in the PHT, the corresponding portion can be quickly searched for in the PHT to determine whether there is a "hit." *See* Specification, page 10, lines 31-36. *See also* Specification, page 11, lines 21-24.

In addition, the XOR circuit performs an XOR operation on only a portion of the instruction address and the contents of a global history register to produce an index. As a result of using only a portion of the instruction address, an unshared index (i.e., a unique index) is generated for each instruction, which prevents or minimizes interference between records of branch outcomes due to shared uses of indexes by different branch instructions. *See* Specification, page 4, line 32 – page 5, line 3. *See also* Specification, page 10, lines 22-27.

Applicants respectfully submit that the Office Action has failed to establish a *prima facie* case of obviousness. In particular, Applicants submit that Henry does not teach or suggest, "a history table ~~which stores therein~~storing a tag, which is a portion of the instruction address," as recited in independent claim 1, for example. Rather, in Henry, an index is obtained by hashing a section of the address. In particular, the index generation logic 312 and 314 include gates for hashing a portion of the address to generate an index into the history tables 302 and 304. Thus, in Henry, unlike in the present invention, time is expended to perform hashing to obtain an index. *See* Henry, column 8, lines 36-40.

Likewise, Shiell does not teach or suggest, "a history table ~~which stores therein~~storing a tag, which is a portion of the instruction address," as recited in newly amended independent claim 1, for example. Rather, Shiell discloses a Branch Target Buffer (BTB), which, according to Shiell, is a cache-like table of entries that each store an identifier for recently-encountered branching instructions. Shiell does not teach or suggest "a tag, which is a *portion* of the instruction address."

Further, Applicants submit that independent claim 1 is also patentable over Henry in view of Shiell, as the references fail to teach "a first count value indicative of a likelihood of branching in association with the first index." In the present invention, if the PHT unit produces a hit, the count value associated with the tag in the PHT unit is updated by incrementing the value by 1 if a branch occurs and decrementing the value by 1 if no branching occurs. *See* Specification, page 14, lines 1-5.

In contrast, Henry teaches update logic including agree or disagree values. For example, in Henry, if a selected dynamic predictor incorrectly predicts a conditional branch instruction outcome, then the selected dynamic predictor is updated by simply "toggling" from its previous value. *See* Henry, column 10, lines 51-52. *See also* Henry, column 11, lines 11-13. *See also* Henry, column 11, lines 28-30. Likewise, Shiell does not teach or suggest a "value indicative of a likelihood of branching in association with the first index." According to Shiell, update occurs through the use of update logic "in the conventional manner." *See* Shiell, column 13, lines 44-47.

In light of the foregoing, Applicants submit that the present invention as defined by independent claim 1 is patentable over Henry in view of Shiell, as the references, taken alone, or in combination, do not render the present invention obvious. Independent claims 6, 7, and 11 recite language similar to that of independent claim 1. Thus, Applicants submit that these claims are patentable over claim 1 for the reasons offered above with respect to claim 1. Dependent claims 2-5 depend from claim 1, and dependent claims 8-10 depend from independent claim 7. Applicants submit that the dependent claims are also patentable over the references for at least the reasons offered above with respect to the independent claims, in addition to other reasons.

For example, dependent claim 2 recites language describing selecting either a first count value or a second value to determine branch prediction and a history table that stores a portion of the address (via claim 1). Applicants submit that the references fail to teach or suggest these features.

Applicants submit that new independent claims 12 and 13 are also patentable over Henry in view of Shiell, as the references fail to teach or suggest using a portion of the instruction address and also fail to teach or suggest a count value as recited in the claims.

Applicants submit that new independent claim 14 is patentable over the references as the references fail to teach, "selecting one of said first count value and said second value to predict branching of said instruction depending upon whether an index is matched to said tag in said first correlation or said tag in said second correlation," as recited in claim 14.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. There being no further outstanding objections or rejections, the application is submitted as being in condition for allowance, which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner's contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 1/27/5

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AMENDMENTS TO THE DRAWINGS:

In the Office Action at item 3, the Examiner objected to the drawings. In order to overcome these objections, replacement figures are submitted herewith. In FIG. 3, labels of operations S1 to S5 are replaced with operations 1-5. Approval of these changes to the Drawings is respectfully requested.